CIRCUIT AND METHOD FOR GENERATING INTERNAL CLOCK SIGNAL

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a circuit and a method for generating an internal clock signal and, more specifically, to a circuit and a method for generating an internal clock signal in a semiconductor memory device, which generates the internal clock signal for synchronizing the operation of the circuit within the semiconductor memory device by using an externally inputted clock signal.

2. Discussion of Related Art

[0002] A device that operates in synchronism with a clock signal employs an external clock signal to generate an internal clock signal whose pulse width is constant for the purpose of a stable operation within the circuit.

[0003] Figs. 1 is a circuit diagram illustrating a circuit for generating an internal clock signal according to a prior art.

[0004] Referring to FIG. 1, the circuit for generating the internal clock signal includes a delay unit 110 and a pulse-shaping unit 120. In the above, the delay unit 110 delays an external clock signal (Ext_CLK) by time corresponding to a desired pulse width. The pulse-shaping unit 120 logically combines a signal (A) that is delayed by given time by the delay unit 110 and

the externally inputted clock signal (Ext_CLK) to generate an internal clock signal (Int_CLK) having a target pulse width (for example, pulse width corresponding to delay time performed in the delay unit).

[0005] Meanwhile, the pulse-shaping unit 120 includes a first NAND gate N121 for performing a NAND operation for the external clock signal (Ext_CLK) and the delay signal (A) of the delay unit 110, a second NAND gate N122 for performing a NAND operation for the external clock signal (Ext_CLK) and the output signal of the first NAND gate N121, and an inverter I121 for inverting the output signal of the second NAND gate N122. At this time, a NAND gate may be further added between the second NAND gate N122 and the inverter I121.

[0006] FIGs. 2A to 2C show internal waveforms for explaining the process of generating the pulse in the circuit for generating the internal clock signal shown in FIG. 1.

[0007] FIG. 2A of them shows a waveform where the delay width of the pulse by the delay unit is smaller than that of the external clock signal. Referring to FIG. 2A, in the event that a delay width (DW) between the delay signal (A) delayed by the delay unit and the external clock signal (Ext_CLK) is smaller than a pulse width (PW) of the external clock signal (Ext_CLK), the internal clock signal (Int_CLK) is normally generated by the logical combination of the logical devices included in the pulse-shaping unit (120 in FIG. 1). In other words, the rising edge of the internal clock signal (Int_CLK) is synchronized to the rising edge of the external clock signal (Ext_CLK). Meanwhile, the pulse width of the internal clock signal (Int_CLK) is set to the

delay width (DW) between the delay signal (A) delayed by the delay unit and the external clock signal (Ext_CLK). Therefore, the pulse width of the internal clock signal (Int_CLK) can be controlled by adjusting the degree of delay of the delay unit.

[0008] Further, FIG. 2B shows a waveform where the delay width of the pulse by the delay unit is coincident with the pulse width of the external clock signal. Referring to FIG. 2B, in case that the delay width (DW) between the delay signal (A) delayed by the delay unit and the external clock signal (Ext_CLK) is coincident with the pulse width (PW) of the external clock signal (Ext_CLK), the internal clock signal (Int_CLK) is normally generated by the logical combination of the logical devices included in the pulse-shaping unit (120 in FIG. 1). In other words, the rising edge of the internal clock signal (Int_CLK) is synchronized to the rising edge of the external clock signal (Ext_CLK). Further, in this case, the pulse width (PW) of the external clock signal (Ext_CLK) is set to the pulse width of the internal clock signal (Int_CLK) as it is.

[0009] Meanwhile, in the event that the delay width (DW) between the delay signal (A) delayed by the delay unit and the external clock signal (Ext_CLK) is greater than the pulse width (PW) of the external clock signal (Ext_CLK), a problem may take place.

[0010] FIG. 2C shows a waveform, in which the delay width of the pulse by the delay unit is greater than the pulse width of the external clock signal. Referring to FIG. 2B, in case that the delay width (DW) between the delay signal (A) delayed by the delay unit and the external clock signal

(Ext_CLK) is greater than the pulse width (PW) of the external clock signal (Ext_CLK), the internal clock signal (Int_CLK) is abnormally generated by the logical combination of the logical devices included in the pulse-shaping unit (120 in FIG. 1). In other words, the rising edge of the internal clock signal (Int_CLK) is not synchronized to the rising edge of the external clock signal (Ext_CLK) and a time point where the internal clock signal (Int_CLK) is enabled according to the frequency of the external clock signal (Ext_CLK) (time point where the rising edge takes place) is differentiated. Further, the pulse width of the internal clock signal (Int_CLK) is set to the width of a High-level portion of the pulse delayed by the delay unit and a portion in which the High level of the external clock signal (Ext_CLK) is not overlapped. The pulse width of the internal clock signal (Int_CLK) can be abruptly reduced depending on the operating frequency (for example, the external clock signal).

[0011] As such, if the time point where the internal clock signal is enabled (for example, the rising edge) is changed depending on the frequency of the external clock signal and the pulse width is abruptly reduced, the operating margin within the circuit is reduced to cause malfunction. This degrades reliability of the circuit and may cause fail even worse.

SUMMARY OF THE INVENTION

[0012] The present invention is directed to a circuit and a method for generating an internal clock signal that can be used in a high frequency and a low frequency at the same time and can improve reliability of the circuit, in

such a way that it is determined whether the external clock signal is the high frequency or the low frequency and the external clock signal is then waveform-shaped to generate the internal clock signal depending on the determination, or the external clock signal as the internal clock signal as it is, thereby making coincident rising edge timings of an external clock signal and an internal clock signal regardless of a frequency of the external clock signal and preventing reduction in an operating margin within the circuit due to reduction in a pulse width of the internal clock signal.

[0013] According to a preferred embodiment of the present invention, there is provided a circuit for generating an internal clock signal, including an operating frequency decision unit for determining whether an external clock signal is a low frequency or a high frequency, and an internal clock signal generator for waveform-shaping the external clock signal and generating an internal clock signal depending on the output of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is.

[0014] In the aforementioned of circuit for generating an internal clock signal according to another embodiment of the present invention, the operating frequency decision unit generates a high frequency to determine whether the external clock signal is the high frequency or the low frequency depending on a CAS latency. At this time, the CAS latency has a value of 0 to 7 and the operating frequency decision unit generates the high frequency if the value of the CAS latency is over 4. Meanwhile, the circuit further includes a mode register for storing the CAS latency.

[0015] The internal clock signal generator includes a delay unit for delaying the external clock signal by some time, and a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is. At this time, the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit.

[0016] The pulse-shaping unit includes a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the output of the operating frequency decision unit, a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted, and an inverter for inverting the output signal of the second NAND gate.

[0017] The delay unit includes a RC delay circuit. The delay unit includes a first inverter for inverting the external clock signal, a number of resistors serially connected between the output of the first inverter and a first node, a number of MOS capacitors connected between the first node and a ground, and a second inverter connected between the first node and an output terminal. Further, the circuit further includes first fuses connected to both ends of the number of the resistors, respectively, wherein the first fuses can be blown, and second fuses connected to the first nodes and the number of the MOS capacitors, respectively, wherein the second fuses can be blown.

[0018] One aspect of the present invention is to provide a method of generating an internal clock signal, including the steps of determining whether an external clock signal is a low frequency or a high frequency, and waveform-shaping the external clock signal and generating an internal clock signal depending on the result of the determination step, or generating the external clock signal as the internal clock signal as it is.

[0019] In the aforementioned of method of generating an internal clock signal according to another embodiment of the present invention, in the determination step, whether the external clock signal is the high frequency or the low frequency is determined as CAS latency. At this time, the CAS latency has a value of 0 to 7 and the external clock signal is determined as the high frequency if the value of the CAS latency is over 4.

[0020] The step of generating the clock includes the steps of waveform-shaping the external clock signal and generating the internal clock signal if the external clock signal is the low frequency, and generating the external clock signal as the internal clock signal as it is if the external clock signal is the high frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] Figs. 1 is a circuit diagram illustrating a circuit for generating an internal clock signal according to a prior art;

[0022] FIGs. 2A to 2C show internal waveforms for explaining the process of generating the pulse in the circuit for generating the internal clock signal shown in FIG. 1;

[0023] FIG. 3 is a circuit diagram illustrating a circuit for generating an internal clock signal according to an embodiment of the present invention;

[0024] FIG. 4 is a circuit diagram for explaining an embodiment of the operating frequency decision unit shown in FIG. 3;

[0025] FIG. 5 is a circuit diagram for explaining an embodiment of the delay unit shown in FIG. 3; and

[0026] FIG. 6 show internal waveforms for explaining the process of generating the pulse in the circuit for generating the internal clock signal shown in FIG. 3.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0027] Now the preferred embodiments according to the present invention will be described with reference to the accompanying drawings. Since preferred embodiments are provided for the purpose that the ordinary skilled in the art are able to understand the present invention, they may be modified in various manners and the scope of the present invention is not limited by the preferred embodiments described later.

[0028] FIG. 3 is a circuit diagram illustrating a circuit for generating an internal clock signal according to an embodiment of the present invention.

[0029] Referring to FIG. 3, the circuit for generating the internal clock signal included in a semiconductor memory device 300 may be implemented using an operating frequency decision unit 310 and an internal clock signal generator 320.

[0030] In the above, the operating frequency decision unit 310 generates a high frequency (HF) depending on the operating frequency (for example, the frequency of the external clock signal) of the semiconductor memory device 300. If the external clock signal (Ext_CLK) corresponds to the HF since it is higher than a given frequency, the operating frequency decision unit 310 activates the HF (defined as a Low level in the present embodiment). The internal clock signal generator 320 waveform-shapes the external clock signal (Ext_CLK) depending on the high frequency (HF) to generate the internal clock signal (Int_CLK), or generates the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) as it is. At this time, if the external clock signal (Ext_CLK) corresponds to a low frequency, the internal clock signal generator 320 waveform-shapes the external clock signal (Ext_CLK) to generate the internal clock signal (Int_CLK). If the external clock signal (Ext_CLK) corresponds to the high frequency, the internal clock signal generator 320 generates the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) as it is. Meanwhile, the waveform shaping of the external clock signal (Ext_CLK) can be accomplished by logically combining the external clock signal (Ext_CLK) and the delay signal (A) of the external clock signal (Ext_CLK).

[0031] As in the above, the operating frequency decision unit 310 determines whether the external clock signal (Ext_CLK) inputted to the semiconductor memory device 300 is the high frequency or the low frequency (for example, in case of about 100MHz, it is the low frequency, and in case of over 500MHz, it is the high frequency). If the external clock signal (Ext_CLK)

is higher than a given frequency, the operating frequency decision unit 310 activates the high frequency. Whether the external clock signal (Ext_CLK) is the high frequency or not could be determined through several methods and constructions accordingly.

[0032] For example, before the memory device 300 is operated, a mode resister set command (MRS command) including signals such as a burst length, a burst type, a column address strobe (CAS) latency and an operating mode is inputted from an external chip set 200, thus deciding the operating mode of the memory device 300. The MRS command is stored at a mode register 330 provided in the memory device 300. At this time, whether the high frequency (HF) has been activated may be decided on the basis of the data for the CAS latency of the MRS command that is inputted from the external chip set 200 and stored at the mode register 330. The CAS latency indicates time latency from a command to output data of a given page is issued until the output is actually performed when any memory cell (page or address block) is activated.

[0033] Generally, the data for the CAS latency consists of 3 bits. As such, the data is composed of the 3 bits, it may have a value from 0 to 7 (000 to 111) depending on the frequency of the external clock signal, as shown in Table 1. At this time, the operating frequency decision unit 310 can determine whether the external clock signal is the high frequency or the low frequency with the data for the CAS latency.

[0034] For example, if the data for the CAS latency is over 4 (100 to 111), it may be set to activate the high frequency (HF) considering that the

external clock signal is the high frequency. In this case, if the data for the CAS latency is over 4 bit, the most significant bit (CL<2>) is always '1' of the data of the 3 bits (CL<0> to CL<2>). Thus, as shown in FIG. 4, the operating frequency decision unit 310 can be implemented only using an inverter I310 for inverting the level of the most significant bit (CL<2>) so that the high frequency (HF) becomes activated (Low level) only when the most significant bit is '1' as a result of sensing only the most significant bit (CL<2>).

□Table 1□

CL<2>	CL<1>	CL<0>	CL Data Value
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

[0035] For example, in case that the high frequency (HF) is outputted by sensing only the data value of the most significant bit (CL<2>), it is possible to implement the operating frequency decision unit 310 using only the inverter for inverting the data of the most significant bit (CL<2>).

[0036] In addition to the above, the basic frequency for deciding whether the external clock signal is the high frequency through the logical combination using the data for the CAS latency.

[0037] Meanwhile, though not shown in the drawings, a frequency sensing means (not shown) of the external clock signal (Ext_CLK) may be located within the memory device 300. The frequency sensing means

compares the frequency of the external clock signal (Ext_CLK) that is externally inputted with the basic frequency to determine whether the frequency of the external clock signal is the high frequency or the low frequency and may activate the high frequency (HF) only when the external clock signal is the high frequency as a result of the determination.

[0038] The internal clock signal generator 320 generates the internal clock signal (Int_CLK) using the external clock signal (Ext_CLK) and, it is determined whether to generate the internal clock signal (Int_CLK) for the low frequency by transforming the external clock signal (Ext_CLK) depending on the high frequency (HF), or to use the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) for the high frequency as it is.

[0039] Such internal clock signal generator 320 may include a delay unit D320 for delaying the external clock signal (Ext_CLK) by some time to generate the delay signal (A), and a pulse-shaping unit P320 for logically combining the external clock signal (Ext_CLK) and the delay signal (A) to generate the internal clock signal (Int_CLK) for the low frequency or transmit the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) for the high frequency as it is if the high frequency (HF) is activated.

[0040] In the above, the delay unit D320 may include a plurality of inverters (only two; IV1, IV2 are shown in the drawing) that are serially connected, for delaying the external clock signal (Ext_CLK) by some delay and then transferring the resulting signal to an inverter connected in a next stage, a plurality of resistors (only two; R1, R2 are shown in the drawing) that

are serially connected between the two inverters IV1 and IV2, and a plurality of MOS capacitors (only three; C1, C2, C3 are shown in the drawing) that are serially in parallel connected between the output terminal of the resistor R2 connected to the final stage of the plurality of the resistors R1 and R2 and the ground terminal, as shown in FIG. 5. The plurality of the resistors R1 and R2 and the MOS capacitors C1, C2, C3 additionally include fuses f1, f2, f3 and f4 that are in parallel connected between respective connecting nodes, so that the connection is selectively controlled depending on blowing of these fuses.

[0041] The delay unit constructed above increases the pulse width if the fuses f1 connected to the resistor is disconnected, while reducing the pulse width if the fuses f2 connected to the MOS capacitor is disconnected. By selectively connecting the resistors and the MOS capacitors connected to the respective fuses by the fuse-blowing mode, it is possible to control the degree of delay accordingly.

[0042] Meanwhile, the pulse-shaping unit P320 may include a first logical means N321 to which the external clock signal (Ext_CLK), the delay signal (A) and the high frequency (HF) are inputted, and a second logical means N322 to which the external clock signal (Ext_CLK) and the output signal of the first logical means N321 are inputted. At this time, if the first logical means N321 or the second logical means N322 consists of a NAND gate, an inverter I321 for inverting the output signal of the second logical means N322 is further installed at the output terminal of the second logical means N322. Meanwhile, though only a single logical means N322 is installed

between the first logical means N321 and the inverter I312 in the drawing, the number of the logical means N322 may be different depending on the case.

[0043] How the internal clock signal generator 320 constructed above operates depending on the high frequency (HF) will now be descried with reference to the waveform. At this time, if the external clock signal is a low frequency, since the high frequency (HF) is generated as a High level (inactive) and thus does not give influence on the operation of the first logical means N321, the internal waveform of the internal clock signal generator 320 is same as that of FIGs. 2A and 2B. At this time, the internal clock signal (Int_CLK) generated becomes the internal clock signal (Int_CLK) for the low frequency. The internal clock signal for the low frequency has the same pulse width as those of the external clock signal but has a pulse width corresponding to the delay time of the delay signal for the external clock signal.

[0044] However, if the external clock signal corresponds to a high frequency and the high frequency (HF) is thus activated as a Low level, they operate quite differently. FIG. 6 show internal waveforms for explaining the process of generating the pulse in the circuit for generating the internal clock signal shown in FIG. 3.

[0045] Referring to FIGs. 3 and 6, if the external clock signal becomes a high frequency, the delay width (DW) between the delay signal (A) delayed by the delay unit D320 and the external clock signal (Ext_CLK) becomes higher than the pulse width (PW) of the external clock signal (Ext_CLK), which may cause a problem. If the external clock signal becomes a high frequency, however, the HF is activated to be a Low level, while the first

logical means N321 becomes a disable state to always output the signal of the High level regardless of the delay signal (A) of the delay unit D320. Therefore, a logical combination of the external clock signal (Ext_CLK) and the delay signal (A) is not performed and the external clock signal (Ext_CLK) are outputted through the second logical means N322 and the inverter I321 as it is. At this time, the external clock signal (Ext_CLK) may be a little delayed by the second logical means N322 and the inverter I321 and the degree of delay is negligible.

[0046] As described above, when the external clock signal is the high frequency, since the external clock signal (Ext_CLK) is outputted as the internal clock signal (Int_CLK) for the high frequency, a problem that the pulse width of the internal clock signal (Int_CLK) is abruptly reduced or a problem that the rising edge is not synchronized can be prevented. It is therefore possible to increase the operating margin and reliability of the circuit.

[0047] According to the present invention, if an external clock signal is a low frequency, an internal clock signal for a low frequency is generated using the external clock signal and a delay signal that delayed the external clock signal. If the external clock signal is a high frequency, the external clock signal is outputted as the internal clock signal for the high frequency as it is. Rising edge time of the external clock signal and the internal clock signal is synchronized regardless of the frequency of the external clock signal and reduction in the operating margin within the circuit due to reduction in the pulse width of the internal clock signal is prevented. It is thus possible to

improve reliability of the circuit while the present invention can be used in the high frequency and the low frequency at the same time.

[0048] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.